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09/751,551	12/28/2000	Jingyu Lian	00 P 9119 US	9195

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SLATER & MATSIL, L.L.P.  
17950 PRESTON ROAD  
SUITE 1000  
DALLAS, TX 75252-5793

EXAMINER

ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/751,551

Applicant(s)  
Lian Et.al.

Examiner  
Edgardo Ortiz

Art Unit  
2815



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Apr 2, 2003
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-13, 21-29, and 31 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13, 21-29, and 31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 17 6) ☐ Other:

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### DETAILED ACTION

This Office Action is in response to a request for continued prosecution filed April 2, 2003 and wherein claims 1, 8 and 28 are amended.

#### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 8, 13 and 21-27 are rejected under 35 U.S.C. § 102 (b) as being anticipated by Nakabayashi (U.S. Patent No. 5,905,278). With regard to Claim 1, Nakabayashi teaches a conductive barrier layer (column 10, lines 38-49) and an electrode (25) comprising a first conductive liner (Ir) disposed over and electrically coupled to the conductive barrier layer, a second conductive liner (IrO<sub>2</sub>) disposed over the first conductive liner, the second conductive liner being electrically coupled to the first conductive liner and the conductive barrier layer and a conductive layer (Ir) disposed over the second conductive liner, the conductive layer being electrically coupled to the first conductive liner, the conductive barrier layer and the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material, see figure 8H.

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With regard to Claim 2, Nakabayashi teaches a second conductive liner ( $\text{IrO}_2$ ) of the lower electrode (25) comprising a conductive oxide.

With regard to Claim 7, Nakabayashi teaches an integrated circuit comprising a FRAM (column 9, lines 48-49).

With regard to Claim 8, Nakabayashi teaches a conductive barrier layer (column 10, lines 38-49) and an electrode (25) comprising a first conductive liner (Ir) deposited over and abutting the conductive barrier layer, the first conductive liner comprising a molecular grain structure having a plurality of columns, a second conductive liner ( $\text{IrO}_2$ ) deposited over and abutting the first conductive liner, the second conductive liner comprising a conductive oxide and a conductive layer (Ir) disposed over and abutting the second conductive liner, the conductive layer comprising a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, this is because of the presence of the conductive oxide between first conductive liner and the conductive layer, see figure 8H.

With regard to Claim 13, Nakabayashi teaches an integrated circuit comprising a FRAM (column 9, lines 48-49).

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With regard to Claims 21 and 22, Nakabayashi teaches a second conductive liner comprising IrO<sub>2</sub>.

With regard to Claims 23 and 24, Nakabayashi teaches a conductive layer and a first conductive liner comprising Ir.

With regard to Claims 25 and 27, the limitation “*wherein the second conductive liner comprises a thickness such that the second conductive liner is etchable by the same etchant used to etch the first conductive liner and the conductive liner*”, is an intended use limitation that does not distinguish the claimed invention from that taught by Nakabayashi. See *In re Pearson* 181 USPQ 641 (CCPA) which makes clear that terms merely setting forth intended use for, or a property inherent in, an otherwise old composition do not differentiate claimed composition from those known to prior art. See also, *In re Swinehart* [169 USPQ 226 ] (CCPA 1971) which makes clear that mere recitation of a newly discovered function or property, inherently possessed by things in prior art, does not cause claim drawn to those things to distinguish over prior art.

With regard to Claim 26, Nakabayashi teaches an electrode (25) having a conductive layer (Ir) comprising a molecular grain structure having columns, the conductive layer including a top surface, wherein the first conductive liner (Ir) comprises a molecular grain structure having columns, wherein the columns of the conductive layer are not aligned with the columns of the first

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conductive liner, this is because of the presence of the conductive oxide ( $\text{IrO}_2$ ) between first conductive liner and the conductive layer.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 5, 9 and 11 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278). Nakabayashi, as stated supra, essentially discloses the claimed invention but fails to show, the thicknesses of the first and second conductive liners. With regard to claims 3, 5, 9 and 11, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include the thickness of the first and second conductive liners as claimed, in order to reduce oxygen diffusion into a conductive layer such as polysilicon below the multi-layer electrode.

Claims 4, 10, 28, 29 and 31 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278) in view of Ramesh (U.S. Patent No. 5,838, 035). With

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regard to Claims 4, 10 and 28, Nakabayashi essentially discloses the claimed invention but fails to show, that the conductive layer and the first conductive liner comprise platinum. Ramesh discloses a capacitor stack with a multi-layer electrode including a barrier layer (72) over a conductive plug (42) of polysilicon, a first conductive layer (74) comprising platinum and a second conductive layer (78) also comprising platinum, see figure 4. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a conductive layer and a first conductive liner wherein both comprise platinum, as clearly suggested by Ramesh, in order to provide an electrode structure which makes use of conductive layers with materials from the precious metals group, which includes both platinum and iridium, known for their conductivity.

With regard to Claim 29, Nakabayashi teaches a second conductive liner comprising  $\text{IrO}_2$ .

With regard to Claim 31, a further difference between the claimed invention and Nakabayashi and Ramesh is, a thickness of the conductive oxide. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi and Ramesh to include a thickness of the conductive oxide as claimed, in order to reduce oxygen diffusion into a conductive layer such as polysilicon below the multi-layer electrode.

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Claims 6 and 12 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278) in view of Yokoyama et.al. (U.S. Patent No. 6,313,539). With regard to Claims 6 and 12, Nakabayashi essentially discloses the claimed invention but fails to show, a barrier layer comprising TaSiN. Yokoyama discloses a semiconductor memory device including a barrier layer (516) comprising TaSiN, see figure 22C. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a barrier layer comprising TaSiN, as clearly suggested by Yokoyama, in order to provide barrier layer comprising a material known for its anti-heat and anti-oxidation properties.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-13, 21-29 and 31 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached by a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general



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nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

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4/30/03



**EDDIE LEE**  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800